REMARKS

Attorney for Assignee thanks the Examiner for the courtesy for the recent interview, the substance of which is incorporated in these Remarks. For the reasons discussed during the interview and which are presented below, and in view of the minor clarifying amendments to Claims 1 and 9, it is respectfully submitted that the cited prior art to Tzeng and Latif can neither anticipate no render obvious any of Claims 1-18 and 24-35. Accordingly, favorable reconsideration of this application and early allowance of all claims is solicited.

As pointed out during the interview, this application relates to storage networks and in particular to storage switches and methods which permit "virtualization" of packets within the switch at wire speed and without buffering the packets. This permits the switch to handle data transfers between initiators, such as servers, and storage devices which store data with minimal delay and at substantially the same rate at which data packets are transferred over the network. The claimed invention accomplishes this by performing the "virtualization" operation on packets at wire speed within the switch and without buffering of the packets within the switch.

The principal points made by Assignee's counsel during the interview, and which are discussed and expanded below, are:

1. Tzeng discloses buffering of packets received and during routing processing for a switching fabric.

2. The specification explicitly defines the terms "virtualization" and "wire speed". These definitions control the interpretation of the claims and preclude the prior art from rendering the claims unpatentable.

3. This Amendment does not raise new issues and is entitled to entry.

A substantial portion of the discussion during the interview focused on U.S. Patent No. 6,693,906 to Tzeng, the primary reference upon which the rejections under 35 U.S.C. §102 and 35 U.S.C. §103 were based, and on Claims 1 and 9. The Examiner had taken the position in the final rejection that Tzeng disclosed the sending and receiving of packets without buffering and at wire speed. In particular, the Examiner's position was that Tzeng discloses receiving at a first port a packet that specifies a virtual target as a destination, and sending at a second port the packet to the physical target associated with the virtual target, where the steps of receiving and sending occur without buffering the packet.

Claims 1 and 9

Claim 1, as amended herein, recites:

> (a) receiving at a first port of the switch a packet that specifies a virtual target as a destination;
>
> (b) sending at a second port of the switch the packet to a physical target that is associated with the virtual target; and
>
> wherein steps (a) and (b) occur without buffering the packet within the switch.

During the interview, it was pointed out to the Examiner that Claim 1 claims a virtualization operation. In order to send the packet received at a first port to a physical target at a second port that is associated with the virtual target specified by the received packet, the sending step (b) of Claim 1 requires that the virtual target

specified by the received packet be associated with a physical target at the second port. The claim cannot be read broadly as merely the steps of "receiving" packets at one port and "sending" packets at a second port, as done by the Office in it's rejection, since this ignores the portion of the sending step of the claim that requires sending the packet to a physical target that is associated with the virtual target specified by the packet, which the claim also requires to be done without buffering.

Tzeng does not disclose (nor suggest) virtualizing packets, as claimed, and indeed, does not even disclose receiving and sending packets without buffering.

Tzeng relates to a network switch and to an Ethernet network, not to a storage switch in a storage network, and that Tzeng's objective to minimize the latency of switched data packets (see column 2, lines 1-2), which he does by providing switching with "a minimal of buffering" (column 1, line 67). In Figure 1 Tzeng illustrates switches 12a-c, each having a switch port 20. The switch port 20 is illustrated in more detail in Figure 3, and comprises everything within the solid lines of that figure. The port also includes a packet classifier module 24 (which is shown within the dotted lines), a MAC module 22, an RxFIFO buffer 27, and a modify header module 29. The RxFIFO 27 is a receive FIFO buffer in the switch port 20 (column 5, lines 37-39) that buffers received data packets. Figure 1 further shows that each switch 12a-c also includes an SSRAM 28 that comprises a buffer memory that "is used by the corresponding switch to store data frames while the switching fabric 25 is processing forwarding decisions for received data packets" (column 3, lines 60-67).

Tzeng relates to an Ethernet that receives different types of data packets, and the reference is primarily concerned with, and the disclosure focuses on, classifying incoming data packets as to data format type, e.g., HTTP, SNMP, etc. Packets are classified as to type at each switch port by the packet classifier module 24 within each switch port, as shown in Figures 1 and 3. Although the packet classifier module is configured for ". . . buffer-free identification (i.e., evaluation) of the incoming data packet at the network switch port 20", and specifies the action to be performed on the data packet based upon the type of data packet received), Tzeng does not disclose either the buffer-free virtualization of packets, or the receiving and sending of packets at switch ports without buffering, as set forth in Claim 1.

Tzeng explicitly discloses that the ports include a received FIFO buffer 27 for received packets (see column 5, lines 36-37), and that the switch 12 includes an SSRAM buffer memory 28 that is used by the switch ". . . to store data frames while the switch fabric 25 is processing forwarding decisions for the received data packets" (column 3, lines 65-67). Thus, Tzeng explicitly discloses buffering packets both when they are received, as well as when performing a virtualization operation by making ". . . forwarding decisions based upon source address, destination address and VLAN information within the Ethernet (IEEE 802.3) header" (see column 3, lines 53-57).

Accordingly, Tzeng does not disclose receiving at a first port of the switch a packet that specifies a virtual target as a destination, where such receiving is done without buffering the packet, as set forth in Claim 1. Furthermore, Tzeng also does not disclose sending the packet to a physical target that is associated with the virtual target specified by the packet at a second port without buffering, since he clearly

teaches the buffer memory 28 for storing data frames while processing forwarding decisions for the received packets.

Accordingly, as was pointed out to the Examiner, and as respectfully submitted here again, Tzeng cannot anticipate Claim 1, even if Claim 1 is read broadly to ignore the virtualization processing in the sending step (b) of associating a physical target to the specified virtual target.

Claim 9

Claim 9 sets forth a method that is substantially the same as that set forth in Claim 1, except that Claim 9 recites that the receiving and sending steps occur at "wire speed", rather than without buffering. As pointed out to the Examiner during the interview, the specification explicitly defines the term "wire speed" at page 6, paragraph [0015] and page 13, paragraph [0062] to mean that the storage switch introduces no more latency to a data packet than would be introduced by a typical network switch that merely performs switching or routing functions, and that the wire speed for a switch is measured by the connection to a particular port, and, thus, the switch has high bandwidth. The specification then goes on to further disclose that in order to process data at wire speed, a storage switch in accordance with the invention will "not buffer packets" as that done conventionally (see paragraph [0015]). Thus, the specification provides an explicit definition for the term "wire speed", and this definition must be used for construing the term "wire speed" in the claims. Tzeng does not disclose or suggest performing virtualization of packets at wire speed, as claimed.

Thus, for the same reasons pointed out in connection with claim 1, Tzeng cannot anticipate Claim 9.

With respect to the Office's position that Tzeng discloses wire speed processing at column 8, lines 52-67, it is respectfully pointed out that Tzeng is referring to performing packet classification with minimal buffering and performing simultaneous processing in order to keep up with the wire rate of incoming packets, ". . . reducing a need for buffering of incoming data . . . by eliminating the need for a large FIFO buffer" (emphasis added). Thus, Tzeng does not disclose virtualization of packets either at wire speed or without buffering, but only with reduced buffering.

During the interview it was noted that independent Claims 1, 10, 12, 24, 30, 32 and 34 all require, in somewhat different ways, virtualization of packets "without buffering the packet", while independent Claims 9, 20, 29 and 31 require virtualization of packets "at wire speed". As pointed out during the interview, the specification explicitly defines the term "virtualization" (at page 14 paragraph [0063]) to mean the "mapping of a virtual target space subscribed to by a user to a space on one or more physical storage target devices".

Claim Terms Defined in the Specification Must Be Construed As Defined

As discussed during the interview, while Patent Examiners give claim terms their broadest reasonable interpretation during examination, where an applicant has provided a definition for a term in the specification, that definition and meaning is controlling and must be ascribed to that term in interpreting the claims. (See *In re Zletz*, 893 F.2d 319, 13 USPQ2d 1320 (Fed. Cir. 1989); *In re Vogel*, 422 F.2d 438, 164

USPQ 619 (CCPA 1970); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 39 USPQ2D 1573 (Fed. Cir. 1996)). Giving a claim term the meaning defined in the specification is not the same thing as the prohibited reading limitations from the specification into the claim to narrow its scope. Rather, it is necessary to comply with the legal standard of allowing an applicant to be his own lexicographer.

As used in the specification and in the claims, virtualization refers to the mapping of virtual target spaces to physical storage target devices. It does not broadly mean, as interpreted by the Examiner, receiving and sending a packet that includes virtual information in the packet header. While the received data packets in Tzeng may include VLAN information within the packet header, receiving and/or sending a data packet with VLAN information in the packet header is not virtualization as that term is defined in the specification and used in the claims. It is respectfully submitted that the Examiner's broad interpretation of the term virtualization and of the virtualization process as claimed, is improper.

Although applicants do not agree with the broad interpretation of Claims 1 and 9 in the Final Rejection that ignores claim limitations, in order to expedite the prosecution of this application, the claims have been amended nevertheless to recite explicitly that which was already implicit in the claims. i.e., that the receiving and sending steps are performed without buffering the packet within the switch, as set forth in Claim 1, and at wire speed within the switch as set forth in Claim 9. Accordingly, it is submitted that Claims 1 and 9 and Claims 2-8 which are depend from Claim 1, are allowable.

Claims 24, 30 and 32

Independent Claim 24 is directed to a storage switch and calls for a processor unit "to perform a virtualization function for the packet without buffering the packet". Claim 30 is directed to a linecard for a storage switch and calls for "means for performing a virtualization function for a packet without buffering the packet"; and Claim 32 is directed to a storage switch and recites "means for receiving at a first port a packet destined for a virtual target and sending the packet to a physical target from a second port without buffering the packet.

As pointed out above, the specification explicitly defines the term "virtualization" to be the mapping of a virtual target space subscribed to by a user to a space on one or more physical storage devices, and that definition must be ascribed to the term "virtualization function" in Claims 24 and 30. As also pointed out, Tzeng explicitly discloses a buffer memory 28 for storing data frames while the switch fabric 25 is processing forwarding decisions for received data packets (column 3, lines 63-67), i.e., performing virtualization. Accordingly, Tzeng does not disclose performing a virtualization without buffering.

Moreover, as previously pointed out, Claims 30 and 32 are written in means plus function format and must be construed in accordance with 35 U.S.C. §112, ¶6 to cover the corresponding structure disclosed in the specification for performing virtualization, and equivalents of that structure. The specification describes the structure performs virtualization as the packet processing unit (PPU) 706 (see pages 18-19, paragraphs [0078]-[0082]). Tzeng does not disclose structure corresponding to

or equivalent to the PPU, , and cannot anticipate Claims 30 and 32 for this reason also.

The rejection of Claim 24 as obvious over the combination of Tzeng and Latif (U.S. Patent No. 6,400,730) is also improper and cannot render the claim obvious since Latif does not disclose performing virtualization on a linecard without buffering, and cannot cure the deficiencies in Tzeng.

The Rejections under 35 U.S.C. §103

As to the rejections of the remaining claims as obvious over the combination of Tzeng and Latif, independent Claims 10, 12, 32 and 34 all call for, in somewhat different ways, virtualization of packets without buffering the packets, and independent Claims 9, 29 and 31 call for, in somewhat different ways, virtualization of packets at line speed.

Latif, as previously pointed out, relates to transferring data over a network between IP network devices and devices using various different data formats, such as SCSI or FIBRE Channel devices. In order to handle the diverse devices, Latif teaches converting a plurality of different input protocols to an internal data format which is used internal for switching between inputs and outputs, and then reconverting the internal format back to an appropriate data format for the device at the output of the switch. Latif discloses buffering of data frames, and does not disclose performing virtualization of packets either without buffering or at wire speed.

As to specific recitations of the claims, Claim 10 sets forth a method for use in a storage switch comprising four steps which are performed by linecards in the switch without buffering. These include:

> (a) receiving at a first port located on a first linecard of the switch a packet that specifies a virtual target as a destination;
>
> (b) the first linecard forwarding the packet to a second linecard of the switch along with information about the virtual target, wherein the second linecard includes a port in communication with a physical target associated with the virtual target;
>
> (c) the second linecard utilizing the information about the virtual target to update the packet with an address of the physical target;
>
> (d) sending by the second linecard the packet to the respective physical target; and
>
> wherein steps (a) - (d) occur without buffering the packet.

All of the recited steps recited in Claim 10, including virtualizing the packet, are performed on first and second linecards in the switch without buffering. Tzeng does not disclose sending, receiving or virtualizing packets without buffering, for the reasons pointed out above.

Independent Claim 12 sets forth a method of virtualizing packets substantially corresponding to that set forth in Claim 10, and is deemed to be allowable for the same reasons Claim 10 is allowable.

Independent Claim 29 is directed to a storage switch and recites, among other things, a processor unit having a virtualization unit to translate at wire speed an address in a packet received at a port from a virtual target address to a physical target address. This is virtualization at wire speed, which the references do not teach or suggest, and is allowable for the same reasons discussed above.

Claim 31 is similar to Claim 29 in calling for a linecard for a storage switch to comprise, among other things, a processor unit that includes a wire-speed virtualization unit. Thus, Claim 31 is also deemed allowable over the references.

Independent Claim 34 is directed to software instructions stored on a medium for use by a storage switch and executable by a processor to perform a series of four steps to perform virtualization, as recited in the claim, all of which are carried out without buffering the packet.

Thus, for the reasons pointed out above, neither Tzeng nor Latif disclose or suggest, individually or in combination, performing virtualization of packets either without buffering or at wire speed, as recited in these claims. Accordingly, these references cannot render any of these independent claims obvious.

Independent Claim 14 is directed to a method for use in a storage switch in which virtualization of packets is performed by an ingress linecard and egress linecard of the storage switch. The claim recites that the ingress linecard places a virtual target descriptor identifier and a flow ID in a local header of the packet and forwards the packet to a fabric which, in turn, forwards the packet to an egress linecard in accordance with the flow ID. The egress linecard uses the virtual target descriptor identifier and information about a physical target to convert a virtual target block address to a physical target block address and sends the packet to the physical target block address, i.e., to perform virtualization. Neither Tzeng nor Latif individually or in combination disclose or suggest the virtualization method set forth in Claim 14 as

performed by ingress and egress linecards of a storage switch. Accordingly, the references cannot render obvious Claim 14 or the claims that depend therefrom.

Claims 19-23 have been allowed, and for the reasons set forth above, Claims 1-18 and 24-34 cannot be anticipated or rendered obvious by the cited prior art. Accordingly, it is respectfully submitted that all claims in this application are allowable and that this application is in condition for allowance.

This Amendment Does Not Raise New Issues and Should Be Entered

During the interview, the Examiner indicated that an amendment to the claims such as presented herein might raise new issues and require a new search. In response, it was pointed out to the Examiner, and is again submitted, that despite the finality of the rejection, the present amendments to the Claims 1 and 9 are minor clarifying amendments which merely make explicit that which was already implicit in the claims, i.e., that the recited steps are performed without buffering or at wire speed within the switch.

Moreover, similar limitations appear the other independent Claims 10, 12, 24, 29, 30, 31, 32 and 34, which have already been searched. Thus, this amendment does not raise new issues which would require a new search, and denial of entry of the amendment on such a basis would be improper.

It is respectfully pointed out that Office policy under compact examination guidelines, as set out in MPEP §904.3, is that Examiners should perform a complete initial search for references that meet not only the terms of broad claims, but that the search should also cover all subject matter that the Examiner reasonably anticipates

might be incorporated into the claims by amendment. That policy presumably was followed here, since the minor amendments to Claims 1 and 9 to emphasize that the recited steps are performed without buffering or at wire speed "within the switch" merely makes explicit that which was already in the claims, are consistent with the arguments that have been made all along, and are similar to the recitations of the other independent and many of the dependent claims.

Accordingly, it is submitted that these amendments do not necessitate a new search, or raise any new issues, and that they are entitled to entry.

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